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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/815,672	04/02/2004	Shiro Dosho	60188-825	9755

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EXAMINER	
LE, DINH THANH	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 06/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/815,672	DOSHO, SHIRO
	Examiner	Art Unit
	DINH T. LE	2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-18 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-18 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 4/2/04 & 9/1/04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

The specification has been checked to the extent necessary to determine the presence of all possible minor errors. However, the applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections

Claim Rejections - 35 USC § 112

Claims 1-18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction or clarification is required.

In claim 1, the recitation "the side" on line 7, "the electric current" on line 16 and "the total voltage" on line 19 lacks clear antecedent basis. It I unclear how the recitation "wherein . . . second electric current" on line 14-17" is read on the preferred embodiment. Insofar as understood, no such limitation is see on the drawings. The same is true for claim 7.

In claim 5, it is unclear what the "normal phase input terminal" and "inverted phase input terminal" of an amplifier are. It is unclear how the recitation "the first . . . reference voltage" on lines 5-9 is read on the preferred embodiment. Insofar as understood, no such limitation is seen on the drawings. The same is true for reciting "second input . . . amplifier" on lines 13-16 of claim 6.

In claim 16, it is unclear how the feedback system can "incorporated" in the upper layer.

In claim 17, it is unclear what the pad region" is and how the feedback system can be "incorporated" in this region.

The remaining claims are dependent from the above claims and therefore also considered indefinite.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-4, 7-8, 10-11, 13-15 and 17 are rejected under 35 USC 102 (e) as being anticipated by Bisanti et al (US 6,600,351). With regard to claims 1-2, 7-8, 10-11, 13-14 and 18, as the best construed, Bisanti et al discloses in Figure 5 a PLL circuit comprising:- a first charge pump circuit (508), a second charge pump circuit (510); a VCO (516) and a loop filter (520). The loop filter (520) including:

- a first element block having a capacitive element (150pF);
- a second element block having a resistive element (60K) coupled in series to the first element block;
- a first input terminal for receiving a first electric current (IR) and being provided at the side of the second element block;
- a second input terminal (512) coupled to a connection point between the first element block and the second element block for receiving a second electric current (Ip); and
- wherein the first element block receives at least a part of the first electric current

(IR)which is corresponds to the difference between the current flowing through the second element block and the second electric current (IR) since the current IR flows in opposite direction to the direction of the current (IP). The total voltage employed as an output signal provided for the VCO (516).

- With regard to claim 3, the second electric current (Ip) flows in an opposite direction to the direction of the first current (IR) and has a magnitude is N time that of the first electric current (IR).

- With regard to claim 4, the recitation "third element block" having a capacitive element is read on the capacitor (56Pf).

- With regard to claims 15, the recitation "the semi conductor integrated circuit is used in an IC card" is considered to be an intended use so that it is not given an patentable weight.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 9 and 16-17 are rejected under 35 USC 103 (a) as being umpatentable over Bisanta et al (US 6,600,351) in view of Maneatis (US 5,727,037). Bisanta et al discloses in Figure 5 a PLL circuit with all of the limitations of the claimed invention as stated above but does not disclose that the VCO (516) is a voltage controlled delay circuit as recited in claim 9, and the circuit of claim 7 is incorporated in an upper layer of the chip-on-chip structure as recited

in claim 16 or in a pad region of an IC as recited in claim 17. Maneatis teaches in Figure 5 a DLL circuit comprising a voltage controlled delay circuit (508) for providing a delayed locked loop. It would have been to a person having skilled in the art at the tie the invention was made to employ the voltage controlled delay circuit taught by Maneatis in the circuit of Bisanta et al for the purpose of forming a delay locked loop. Also, the PLL/DLL circuit is used as a signal source for an integrated circuit (CHIP) is suggested in Maneatis, see Figure 7. A skilled artisan realized that the PLL circuit of Bisanta et al can be arranged within the IC to accommodate with the physical size and shape of the IC in which the PLL circuit is to be used. Thus, incorporating the PLL circuit of Bisanta et al in an upper layer or in a pad region of the IC is considered to be a matter of a mechanical design expedient for an engineer. Lacking showing any criticality, it would have been obvious to a person having skill in the art at the time the invention was made to incorporate the PLL circuit of Bisanta et al in an IC as claimed for the purpose of accommodating with the physical size and shape of the IC.

Allowable Subject Matter

Claim 6 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

Claims 5 and 12 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

The claims are allowed because the prior art does not show the operational amplifier as combined in claims 5-6 and the first input terminal is provided at the side including the first

element block as recited in claim 12.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DINH T. LE whose telephone number is (571) 272-1745. The examiner can normally be reached on Monday-Friday (8AM-7PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, TIMOTHY CALLAHAN can be reached at (571) 272-1740.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DINH T. LE
PRIMARY EXAMINER